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(54) Self oscillating power amplifier

(57) A power amplifier includes a comparator (COMP) to which an input signal is applied, a digital buffer (BUF) coupled via a feedback low-pass filter (LPFB) to a second input terminal (Cin2) of said comparator (COMP). An unstable loop is thereby created with an oscillation frequency related to the bandwidth of the

feedback low-pass filter. In the presence of an input signal this self-oscillation frequency linearizes the system resulting in a power amplifier with excellent power efficiency. In a differential version two of these self-oscillating loops are provided. The coupling of the two loops thereby withholds the high-frequency self-oscillation from the load.

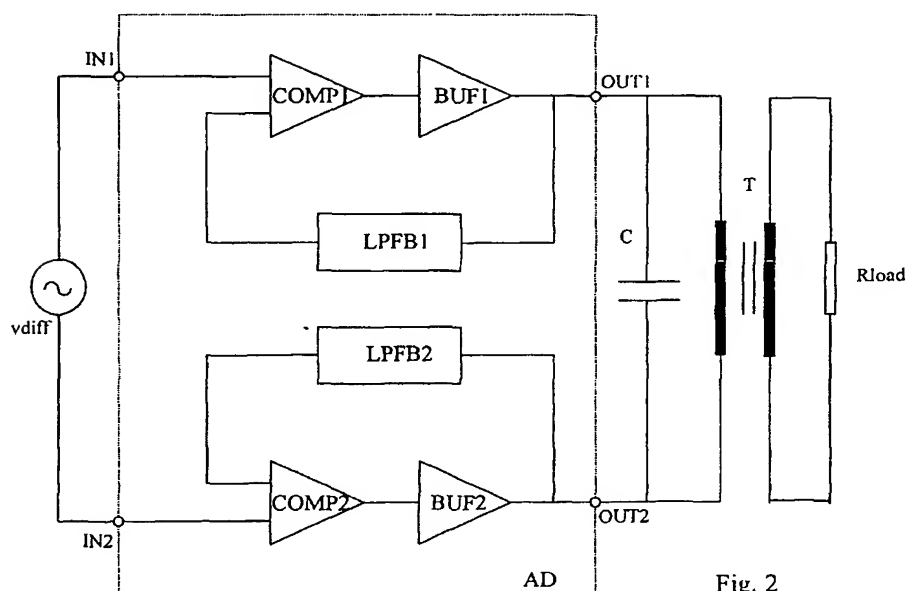


Fig. 2

EP 1 229 641 A1

Description

[0001] The present invention relates to a power amplifier as is described in the non-characterising portion of the first claim.

[0002] Such a power amplifier is already known in the art, e.g. from the article "An IC for Linearizing RF Power Amplifiers using Envelope Elimination and Restoration", by D. Su and W. McFarland, ISSCC 1998 Technical Digest, paper 3.6-2. Therein, in Fig. 2a, a circuit is shown wherein a comparator in series with a Class-D buffer and a lowpass filter is coupled to a resistive load, this circuit having a direct feedback from the output to the input of the system.

[0003] A drawback of such a circuit is that its operation is based on switch-capacitors, which obviously need to be clocked, as is clearly shown in Fig. 2b. The presence of such a high-frequency sampling clock however seriously increases the power consumption. This seriously hampers its use in especially xDSL systems, where the power consumption of the output amplifier, is a serious issue.

[0004] An object of the present invention is to provide a power amplifier of the above known type but which has a much better power efficiency compared to the prior art circuit.

[0005] According to the invention, this object is achieved due to the presence of a low-pass filter in the feedback loop of the amplifier arrangement, as is further described in the characterising portion of the first claim.

[0006] In this way, by inserting a low-pass filter in the feedback path, an unstable feedback loop is created, with an oscillation frequency related to the bandwidth of this low-pass filter. This limit cycle oscillation within the loop results in the square wave at the output with this oscillation frequency. When this unstable system is forced by an external signal V_{in} at the input of the comparator, having a frequency lower than this self oscillation frequency, this self-oscillation or limit cycle oscillation acts as dither and linearizes the system as long as the differential or error signal between the inputs of the comparator is smaller than the limit cycle amplitude at the comparator input. The output is a square wave containing the self-oscillation frequency and the amplified forced signal. With limit cycle amplitude is meant the amplitude between the inputs of the comparator in the case no external input signal is present.

[0007] Since this amplifier is a switching type amplifier a high efficiency can be obtained, even when buffering signals with a high crest factor as in xDSL. Since, in comparison to the prior art system no clock is used, power efficiency is seriously improved.

[0008] Another characteristic feature of the present invention is described in claim 2.

[0009] In this way, by inserting an additional low-pass filter between the output of the amplifier arrangement and the load, the high-frequency modulation components are filtered out.

[0010] A further characteristic feature of the present invention is described in claim 3.

[0011] This means that the minimum self-oscillation frequency, which is mainly determined by the cut-off frequency of the low pass filter in the feedback path, merely has to be a factor 3 larger than the bandwidth of the input signal to be amplified. In the already mentioned prior art systems, the switching or clock frequency has to be generally more than a factor 10 larger than the bandwidth of the input signal to obtain enough suppression of the quantisation noise. This is because in the prior art system the signal is presented by a discrete amplitude, discrete time signal while in the present amplifier it is a discrete amplitude, continuous time signal. This presents an additional advantage of the present amplifier with respect to higher obtainable bandwidths.

[0012] Claim 4 describes the differential version of the output amplifier arrangement.

[0013] Compared to the single-ended version, the differential structure provides power supply modulation rejection and better noise immunity. This adds to the maximum Signal to Noise ratio attainable in the present amplifier.

[0014] A gain in efficiency is obtained since the two oscillation loops are attracted towards each other. As such the main switching frequency is not transferred to the load, since it becomes common mode for the load. This again adds to the power efficiency.

[0015] Yet a further characteristic feature of the present invention is mentioned in claim 7.

[0016] By the coupling of the load via a transformer, the high frequency common mode component can completely be filtered out, and the load is galvanically decoupled from the amplifier.

[0017] Still another characteristic feature of the present invention is mentioned in claim 8.

[0018] The presence of the capacitor improves the coupling between the two oscillation loops and leads to a better signal integrity. Furthermore the combination of this capacitor and the transformer will result in a lowering of the series impedance of the windings of the transformer coils, again improving the efficiency of the amplifier.

[0019] The above and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wherein:

FIG. 1 represents a schematic of a single ended amplifier arrangement AS of the invention,
 Fig. 2 represents a schematic of a differential amplifier arrangement AD of the invention, and
 Fig. 3 gives a transistor level embodiment of the different blocks shown in Fig. 1 and Fig. 2 , and

Fig. 4 represents the output spectrum measured on a differential structure as in Fig. 2, using embodiments of the building blocks as in Fig. 3.

[0020] A single ended schematic of an output amplifier arrangement AS of the present invention is shown in Fig. 1. This amplifier arrangement includes an input terminal IN to which an input signal v_{in} can be supplied. The input terminal IN is coupled to a first input terminal Cin1 of a comparator COMP. This comparator has a second input terminal Cin2, and is further adapted to compare input signals supplied to both input terminals with each other. The result of this comparison is delivered to the output terminal Cout of the comparator, which is further coupled to the input terminal Bin of a digital buffer BUF. The latter amplifies the digital input signal present at Bin, for delivery of the amplified signal at its output terminal Bout, which is further coupled to the output terminal OUT of the output amplifier arrangement AS. Bout is also coupled in a feedback loop to the second input terminal Cin2 of the comparator, via a feedback low-pass filter LPFB. Bout is thus coupled to input terminal LPFBin of LPFB, whereas an output terminal LPFBout of this low-pass filter is coupled to Cin2. The amplifier arrangement AS will deliver power to a load RLOAD, via the coupling of the output terminal OUT of the amplifier arrangement AS to a terminal of this load impedance. In the embodiment shown in Fig. 1 a second low-pass filter LPS is shown in between the buffer output terminal Bout and the output terminal OUT of the amplifier arrangement. The functionality of the amplifier arrangement AS will however first be explained for an embodiment without this second low-pass filter LPS.

[0021] The feedback low-pass loop filter LPFB is constructed in such a way that the loop is unstable, also in the presence of an input signal. This is realised by carefully choosing the cut-off frequency and the order of the low-pass filter such that the self-oscillation frequency, which is the frequency at which the system oscillates without an external input signal present, is at least 3 times larger than the bandwidth of the input frequency of the system. This consideration can for instance be found within tutorial handbook "Multiple-input describing functions and non-linear system design", written by A. Gelb and W. Vander Velde, Mc-Graw-Hill Book Company, 1968. In this case, the instability is also preserved in the presence of an input signal. Therefore the loop will also oscillate, with this self-oscillation frequency, hereafter called the limit cycle frequency, in the presence of an input signal v_{in} . In this condition the limit or oscillation cycle acts as dither and linearizes the system as long as the error signal between the two inputs of the comparator COMP is smaller than the limit cycle amplitude at the comparator input. In that case the output is a square wave containing the limit cycle frequency and the driving input signal. With limit cycle amplitude is meant the amplitude between the inputs of the comparator in the case of no external input signal present.

[0022] In order to filter out these high-frequency oscillation components, a second low-pass filter can be coupled in between the buffer output terminal Bout and the output terminal OUT of the amplifier arrangement.

[0023] The transfer function of the linearized system is dependent on the limit cycle amplitude. This can be understood from the following mathematical considerations:

The system consisting of the comparator COMP, the buffer BUF and the feedback filter LPFB, can be analyzed by making use of the describing functions approach. In this approach the comparator COMP followed by the digital buffer BUF can be modeled by the following describing function $N'(A)$.

$$N'(A) = N(A) \frac{p_1}{s + p_1}$$

Herein p_1 is the first order pole of the comparator and $N(A)$ is a complex gain, dependent on the input amplitude A . This gain can be calculated using the following equation

$$N(A) = \frac{j}{\pi A} \int_0^{2\pi} y(A \sin \psi) e^{-j\psi} d\psi$$

Which results in:

$$N(A) = \frac{2V_{DD}}{\pi A}$$

for an ideal comparator COMP and only one frequency ω_0 present in the loop with an amplitude A . From this the limit cycle amplitude and frequency can be calculated, by solving the following complex equation:

EP 1 229 641 A1

$$1 + N(A)LPFB(s) = 0$$

Since this is an inherent nonlinear system, these equations cannot be used to calculate the systems response on an input signal v_{in} at the input IN. This because the superposition principle no longer holds. To analyze this a Two-Sinusoid Describing Function has been calculated.

$$N'_2(A, e) = N_2(A, e) \frac{p_1}{s + p_1}$$

N'_2 represents the comparator COMP by a dominant pole p_1 and a complex gain N_2 dependent on the limit cycle amplitude A and the error signal e amplitude between $cin1$ and $cin2$ which occurs when the input signal v_{in} is applied at the input IN. This complex amplitude can be calculated as follows :

$$N_2(A, e) = \frac{j}{\pi e} \int_{-\infty}^{\infty} \mathcal{F}(y(x)) J_0(A.u) J_1(e.u) du$$

with $\mathcal{F}(y(x))$ being the Fourier Transform of the DC transfer characteristic $y(x)$ of the comparator. J_0 is the Bessel function of the first kind of order 0. J_1 is the Bessel function of the first kind of order 1. Solving this equation using the Fourier transform of an ideal comparator:

$$\mathcal{F}(y(x)) = \frac{V_{DD}}{ju}$$

yields :

$$N_2(A, e) = \begin{cases} \frac{V_{DD}}{\pi e} \left(\frac{e}{A} \right) {}_2F_1\left(\frac{1}{2}, \frac{1}{2}; 2; \left(\frac{e}{A}\right)^2\right) & \text{for } 0 < e < A \\ \frac{2V_{DD}}{\pi e} {}_2F_1\left(\frac{1}{2}, -\frac{1}{2}; 1; \left(\frac{A}{e}\right)^2\right) & \text{for } 0 < A < e \end{cases}$$

$$\approx \frac{N(A)}{2} \quad \text{when } 0 < e \ll A$$

With ${}_2F_1$ the hypergeometric function with a second order nominator and a first order denominator. When $e < A$, ${}_2F_1$ becomes 1, making the transfer function independent on the input signal, thus lowering the distortion. This equation puts a limit on the maximum output voltage when a certain distortion level is required. The transfer function of the complete system consisting of COMP, BUF and LPFB thus becomes :

$$T(s) = \frac{N_2(A, e)}{1 + N_2(A, e)LPFB(s)}$$

From this one can suggest self-adaptivity to the system. Since a changing load condition, affects the input-output characteristic of the digital driver, the limit cycle amplitude and frequency is changed. However since the transfer function of LPFB is not affected the transfer function of the complete system for a forced signal is not changed.

[0024] Since it also became clear that the limit cycle amplitude depends on the load coupled to the digital buffer, the complete system becomes self-adaptive to load variations. This effect becomes less pronounced in the presence of an extra low-pass filter LPS for filtering out the self-oscillation frequency.

[0025] Fig. 2 shows the differential version of the amplifier arrangement of the present invention. This embodiment mainly consists of two similar loops as described in the first embodiment : a first loop consisting of comparator COMP1, digital buffer BUF1 and low-pass filter LPFB1, and a second loop consisting of comparator COMP2, digital buffer BUF2

and low-pass filter LPFB2. The first loop is coupled to a first differential input terminal IN1 of the differential amplifier arrangement AD, whereas the second loop is coupled to a second differential input terminal IN2 of the differential amplifier arrangement AD. In between both differential input terminals IN1 and IN2, a differential input signal v_{diff} , can be applied. The differential power amplifier arrangement AD includes a pair of differential output terminals : OUT1 and OUT2, to which the two terminals of the load impedance RLOAD can be coupled. Both loops contain similar components such that the limit cycle oscillation frequencies of both loops are the same

[0026] The operation of this differential version AD is similar to the operation of the single-ended version AS, in the sense that both individual loops will oscillate at the same limit cycle oscillation frequency. Also in this case the bandwidth of the input signal has to be at least a factor 3 smaller than the self-oscillation frequency of the loops.

[0027] By means of the coupling of the two oscillation loops via the load, the oscillators are attracted towards each other, forcing the limit cycles to oscillate in phase. Therefore merely the amplified input signal is transferred to the load, while the high frequency oscillation is withheld from this load. The differential structure thus provides power supply modulation rejection. Since the limit cycle frequency is not transferred to the load, there is no need to add an additional low-pass filter in series, as was the case for the single-ended embodiment of fig. 1.

[0028] The attraction between both oscillation loops may be enforced by the presence of an inductive coupling, such as realised by means of a transformer T in parallel with the load, as is also shown in Fig. 2. In that way the limit cycle will become common mode for the primary winding of the transformer. Since this is decoupled from the load by the transformer itself, common mode rejection ratio is improved. Noise immunity is thereby improved. It is to be noted that for applications of DSL output amplifiers, such transformers are present for decoupling the line, such that they do not need to be separately provided.

[0029] A capacitor C can also be coupled between the two differential output terminals, as is also shown in Fig. 2. A capacitor has the advantage of providing a low impedance, which facilitates the attraction between the two loops. In combination with the aforementioned transformer T this capacitor will reduce the high inherent impedance of the transformer.

[0030] Fig. 3 shows detailed embodiments at transistor level of the different components of Figs 1 and 2. The loop filters LPFB, LPFB1 and LPFB2 have been realised as a third order RC filter, denoted "feedback filter" on fig. 3, for keeping a high linearity in the feedback circuitry. To reduce the transfer time through the comparator a 3-stage structure has been chosen for COMP, COMP1 and COMP2, using positive feedback to ensure a rapid comparison followed by a self-biasing post amplifier. This is all contained in the block denoted "Comparator" in Fig. 3. To prevent large shoot-through currents during switching a non-overlapping switching circuit was added. The delay of this non-overlapping signal scheme is combined with a digital buffer to reduce the rise time of the large output driver. The transistors contained in the block denoted "digital buffer combined with no DC current circuit" together with those in the block "output driver" all form together an embodiment of the digital buffer BUF of Fig. 1 and of BUF1 and BUF2 of Fig. 2.

[0031] As can be seen from fig. 3, this amplifier can be realised using CMOS technologies. In a particular embodiment for realising the scheme of Fig. 2, the circuits of Fig. 3, implemented in a 0.35 μm CMOS technology, an standard transformer T and a standard coupling capacitor C, were used. This complete circuit has been proven feasible to drive any load down to 2.4 Ohm. This is important with respect to the scaling of technology. Indeed, when used as DSL output amplifier, the signal levels on the line tend to remain the same magnitude (15 V), while the supply voltage drops with every technology generation. Transformers are used to overcome this problem and to make a galvanic isolation. Yet the resistance is then decreased by the square of the transformer ratio.

[0032] For a supply voltage of 3.3 V, a resistive load of 2.4 Ohm, a linear audiocapacitor of 40 nF and a ADTT1-6 transformer with a ratio of 1:1, an output voltage of 1.2 V peak-to-peak, a voltage gain of 0.9 and an efficiency of 48 % were obtained for an input signal of 1.3 V peak-to-peak. It has to be noted that this efficiency includes the losses of the used transformer. If the transformer losses are calibrated out, an efficiency of 61 % is achieved. It is important to notice that the efficiency drops sub-linear, resulting in a better efficiency than that of an ideal class B amplifier for input signals with a crest factor higher than 1.2.

[0033] Fig. 4 shows the output spectrum up to 20 MHz, of the thus realised differential amplifier structure with transformer and coupling capacitor. An input signal of 200 kHz was applied. The self-oscillation frequency was equal to 3.8 MHz. From this figure it is clear that due to the coupling of both loops the self-oscillation frequency and its harmonics are suppressed. This figure hardly changes for higher signal frequencies up to about 1 MHz. For a 800 KHz input signal a 54.4 dB spurious free dynamic range, abbreviated with SFDR is measured. For a 900 kHz input signal, the SFDR has decreased to a level of 51.2 dB. For higher signal frequencies the linearizing effect drops drastically, since in that case the condition stating that the bandwidth of the input signal has to be at least three times smaller than the self-oscillating frequency, is no longer fulfilled.

[0034] While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention, as defined in the appended claims.

Claims

1. Power Amplifier arrangement (AS) including an input terminal (IN) for coupling to an input signal (vin) source, said amplifier arrangement further including a comparator (COMP), a first input terminal (Cin) of which is coupled to said input terminal (IN) of said amplifier arrangement, an output terminal (Cout) of which is coupled to an input terminal (Bin) of a digital buffer (BUF) of said amplifier arrangement, a buffer output terminal (Bout) of said digital buffer being coupled to an output terminal (OUT) of said amplifier arrangement (AS) and to a second input terminal (Cin2) of said comparator (COMP)
characterized in that
said buffer output terminal (BOUT) is coupled via a feedback low-pass filter (LPFB) of said amplifier arrangement (AS), to said second input terminal (Cin2) of said comparator (COMP).
2. Power amplifier arrangement (AS) according to claim 1
characterized in that
said buffer output terminal (Bout) is coupled to said output terminal (OUT) via a second low-pass filter (LPS) of said amplifier arrangement (AS).
3. Power amplifier arrangement (AS) according to claim 1
characterized in that
the bandwidth of said input signal (vin) is at least three times smaller than the self-oscillating frequency of said power amplifier arrangement.
4. Differential power amplifier arrangement (AD) including a pair of differential input terminals (IN1,IN2) to which a differential input voltage (vdiff) can be applied, and a pair of differential output terminal (OUT1,OUT2) for coupling to a load (Rload)
 - said differential power amplifier arrangement including a first self-oscillating loop with an input terminal coupled to a first one (IN1) of said pair of differential input terminals, said first self-oscillating loop including a first comparator (COMP1) coupled to a first digital buffer (BUF1), an output terminal of which is coupled to a second input terminal of said first comparator via a first low-pass filter (LPFB1),
 - said differential power amplifier arrangement including a second self-oscillating loop with an input terminal coupled to a second one (IN2) of said pair of differential input terminals, said second self-oscillating loop including a second comparator (COMP2) coupled to a second digital buffer (BUF2), an output terminal of which is coupled to a second input terminal of said second comparator via a second low-pass filter (LPFB2).
5. Differential power amplifier arrangement (AD) according to claim 4
characterized in that
said first self-oscillating loop is substantially identical to said second self-oscillating loop.
6. Differential power amplifier arrangement (AD) according to claim 5
characterized in that
the bandwidth of said differential input signal (vdiff) is at least three times smaller than the self-oscillating frequency of said differential power amplifier arrangement (AD).
7. Differential power amplifier arrangement (AD) according to claim 4,
characterized in that
said load is coupled to said pair of differential output terminals via a transformer, a primary winding of which is coupled between said pair of differential output terminals (OUT1, OUT2), a secondary winding of which is coupled in parallel to said load.
8. Differential power amplifier arrangement (AD) according to claims 4 or 7
characterised in that
said load is coupled in parallel with a capacitor (C), which is coupled between said pair of differential output terminals (OUT1,OUT2).

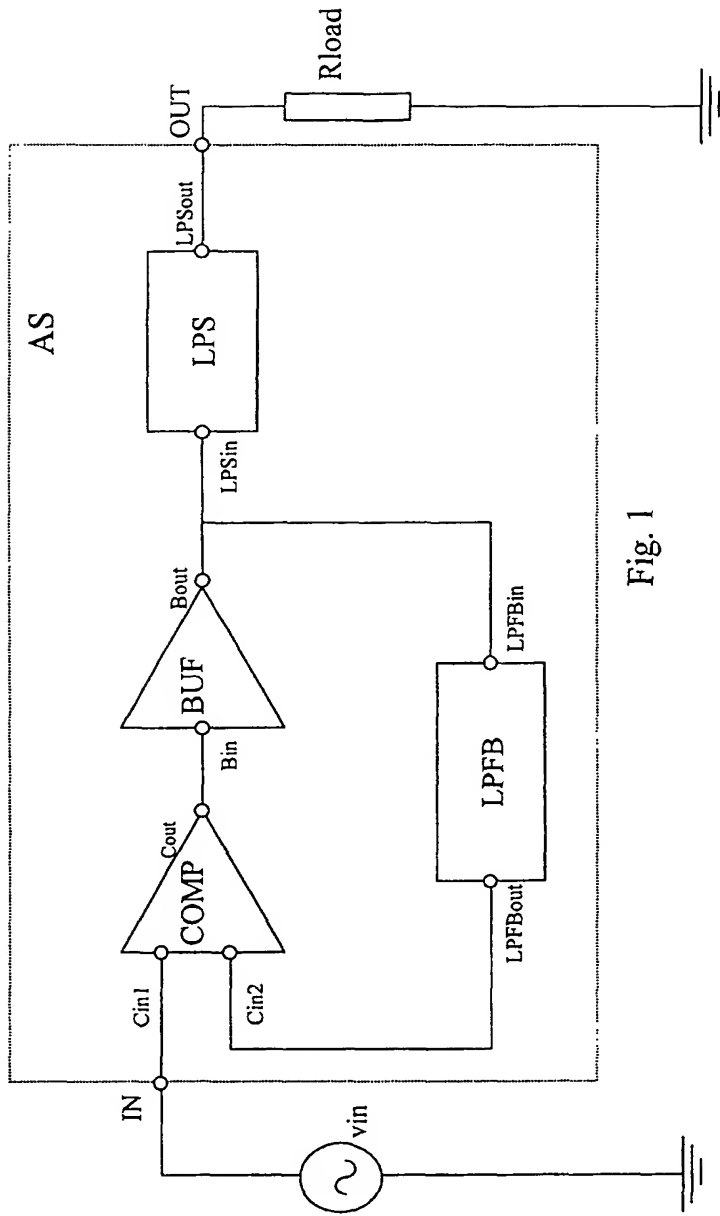


Fig. 1

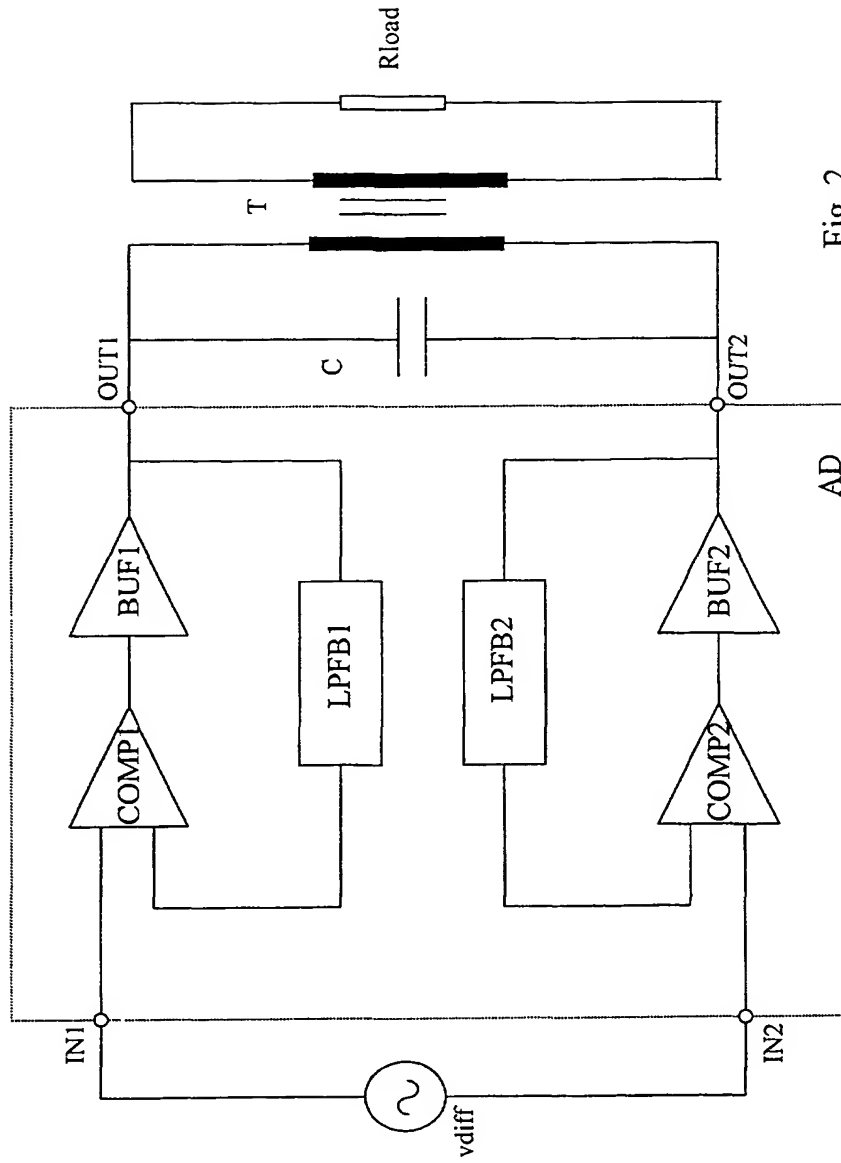


Fig. 2

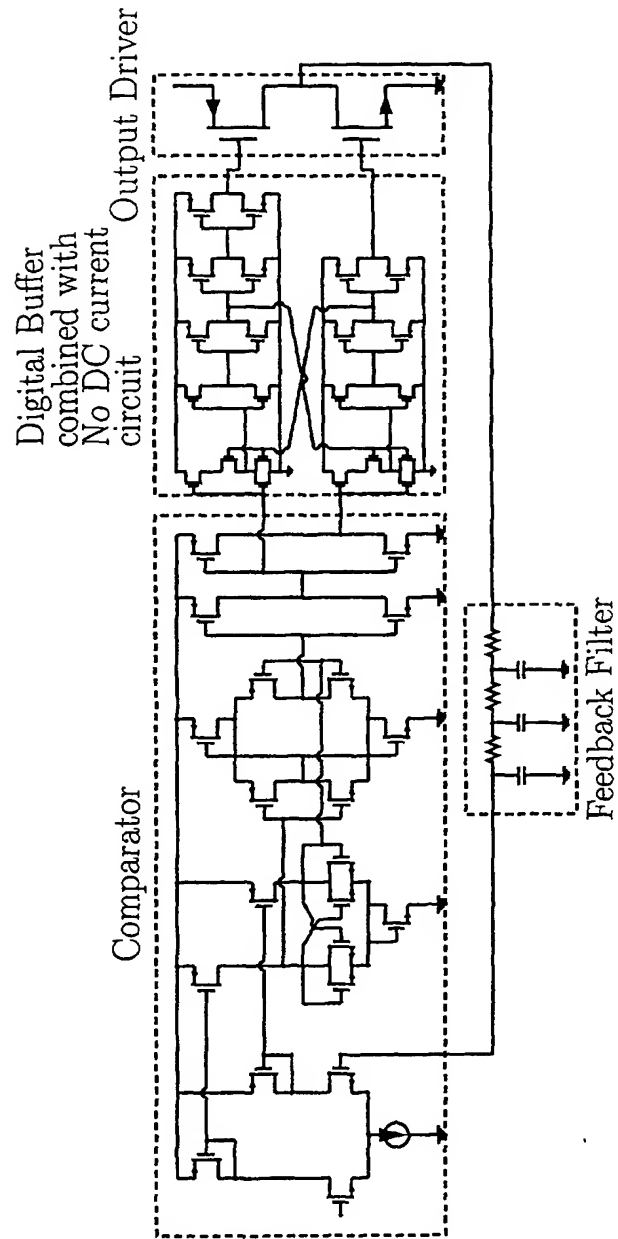


Fig. 3

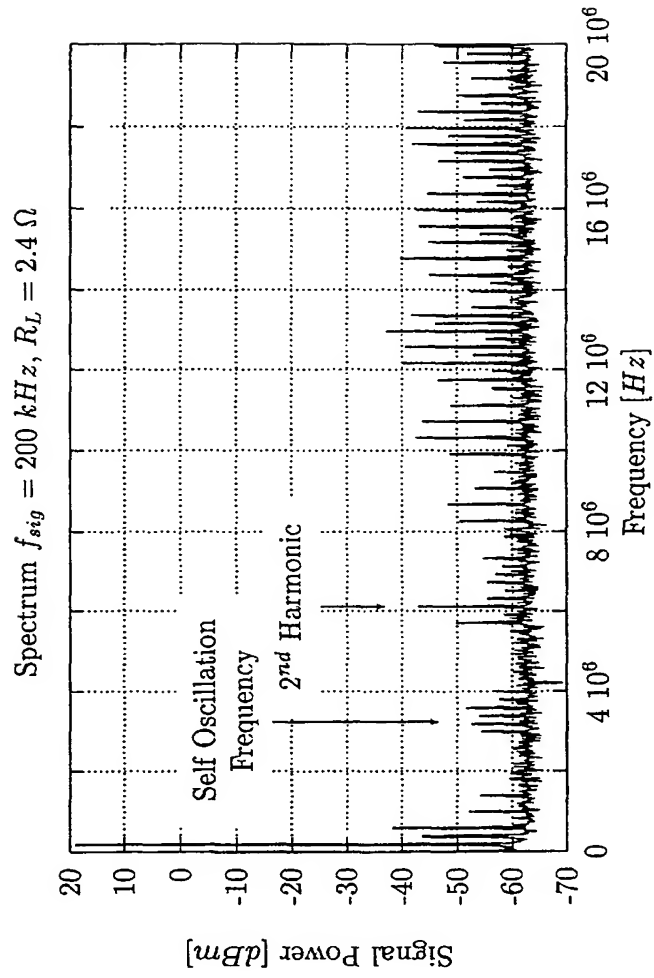


Fig. 4

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EUROPEAN SEARCH REPORT

Application Number
EP 01 40 0257

DOCUMENTS CONSIDERED TO BE RELEVANT					
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)		
X	WO 98 19391 A (BANG & OLUFSEN AS ;KARSTEN NIELSEN (DK)) 7 May 1998 (1998-05-07) * page 15, line 27 - page 16, line 22; figure 10 *	1-3	H03F3/217		
Y	* page 19, line 4 - line 10; figure 8 * * page 8, line 18 - page 9, line 9; figure 4 *	4-8			
Y	----- SHERMAN J D: "CLASS D AMPLIFIERS PROVIDE HIGH EFFICIENCY FOR AUDIO SYSTEMS" EDN ELECTRICAL DESIGN NEWS,US,CAHNERS PUBLISHING CO. NEWTON, MASSACHUSETTS, vol. 40, no. 11, 25 May 1995 (1995-05-25), pages 103-106,108,11, XP000520335 ISSN: 0012-7515 * page 3; figure 4 *	4-6			
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D,A	----- D. SU W. MCFARLAND: "An IC for linearizing RF power amplifiers using envelope elimination and restoration" IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE., 5 - 7 February 1998, pages 3.6-1-3.6-9, XP002169050 IEEE INC. NEW YORK., US ISSN: 0193-6530 * page 3.6-1, left-hand column, line 45 - line 61; figure 2 *	1-3	<table border="1"> <thead> <tr> <th>TECHNICAL FIELDS SEARCHED (Int.Cl.7)</th> </tr> </thead> <tbody> <tr> <td>H03F</td> </tr> </tbody> </table>	TECHNICAL FIELDS SEARCHED (Int.Cl.7)	H03F
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The present search report has been drawn up for all claims					
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EP 1 229 641 A1

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EP 01 40 0257

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